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(54) [Title of the Invention]: Transformer Drive Circuit

(57) [Abstract]

[Object] It is to configure a transformer drive circuit such that, even when a plurality of switching circuit sections are installed, a sum of values of ripple currents that flow into electrolytic capacitors each constituting the respective switching circuit sections does not increase in comparison with a ripple current value flowing in a circuit comprising one switching section and such that the transformer drive circuit can be operated with a minimum requisite capacity of the electrolytic capacitors.

[Means for solving Problem]

A timing generator 15 generates a plurality of clock

signals having phases being different from one to another based on clock signals generated by a clock generator 14 and supplies the clock signals to switching transistors Q1 to Qn, respectively. Switching transistors Q1 to Qn performs tuning on and off operations in response to the respective clock signals to excite the transformers T1 to Tn. An averaged ripple current is supplied to the electrolytic capacitor.

[Claims]

[Claim 1] A separately-excited transformer drive circuit for excitingly driving a plurality of transformers characterized in that the circuit comprising;

a plurality of transformers each being connected to one electric power source,

a plurality of capacitors being installed correspondingly to the plurality of transformers, each performing the commutation and smoothing of a voltage to be inputted to the corresponding transformer and performing energy supply and storage to/from the corresponding transformer,

switching transistors respectively installed correspondingly to the plurality of transformers to drive the corresponding transformer,

a clock generating means for generating at least one clock signal, and

a timing control means for generating a plurality of clock signals, phases of those which being different from one to another, based on the clock signals generated by the clock generating means.

[Claim 2] A transformer drive circuit according to claim 1 wherein,

the clock generating means generates one clock signal, and

the timing control means equally divides the cycle T of the transformer drive into n portions to obtain a time period of T/n and delays the clock signal stepwise by the time period of T/n to produce n pieces of clock signals and supplies the divided signals respectively to the corresponding switching

transistors.

[Claim 3] A transformer drive circuit according to claim 1, wherein the clock generating means generates a plurality of clock signals having phases being different from one to another.

[Claim 4] A transformer drive circuit according to any one of claims 1 to 3, wherein a high voltage generated by each of the plurality of transformers is supplied to an image forming apparatus.

[Detailed Explanation of the Invention]

[0001]

[Field of the Invention]

The present invention relates to a separately-excited transformer drive circuit and particularly to a separately-excited transformer drive circuit to be used for an image forming apparatus, such as a laser printer, a copying apparatus and a facsimile apparatus, that employs the electronic photography processing mode.

[0002]

[Prior Art]

In general, an image forming apparatus employing the electronic photography processing mode is provided with a high-voltage generating apparatus, and the high-voltage generating apparatus basically produces a primary electrification bias, a development bias, a transfer bias, a fixation bias and the like those which are required in an image forming apparatus.

[0003]

With the tendency of coloring image forming apparatuses,

high-voltage biases to be required are getting sophisticated, making a plurality of manifold biases to be required. For example, in a color printer that is configured such that a transfer material such as a paper is adsorbed onto a transfer drum or a transfer belt, a toner is transferred onto the transfer material, and the transfer material is then separated and fixed, an adsorption bias, an antistatic separation bias and the like are required.

[0004]

Besides, in a color laser printer in which an intermediate transfer body is contained, toner images developed on an image carrier are transferred in turn for the respective colored components of yellow, magenta, cyan and black and then secondarily transferred onto the transfer material in the block. Hence, it is required for the transfer bias a primary transfer bias for transferring a toner image from the image carrier to the intermediate transfer body and a secondary transfer bias for transferring the tone image once more from the intermediate transfer body to the transfer material.

[0005]

Further, in a high-speed color laser printer, there is a case where four latent image forming processes and four development processes are independently configured for the respective colors. In such a case, four primary electrification biases and four development biases are also required frequently. In this way, the configuration of the high-voltage bias is getting complex and diverse with the tendency of coloring image forming apparatuses.

[0006]

Now, the configuration of a transformer drive circuit of the conventional type to be used for a high-voltage generation apparatus will be explained.

[0007]

FIG. 5 is a block diagram showing the transformer drive circuit used in a conventional high-voltage generation apparatus.

[0008]

In this figure, a plurality of switching circuit sections (1 to n) 51 to 53 are provided in the transformer drive circuit, and these switching circuits are respectively driven in a separately-excited manner by one clock generator 54. Note that n is an integer of 2 or more. The clock generator 54 generates a clock signal with a predetermined frequency and duty. The generated clock signal is commonly supplied from the switching circuit section (1) 51 to all of the switching circuit sections, that is till the switching circuit section (n) 53, whereby the respective switching circuits excitingly drive the respective transformers T1 to Tn.

[0009]

The respective transformer T1 to Tn is structured to contain bifilar windings at the input coil winding sides thereof, and diodes D1 to Dn and coil windings a1 to an form snubber circuits, respectively. The respective common terminals of the coil windings are connected respectively to an electric power source (+24V) and electrolytic capacitors C1 to Cn. Wave forms of currents flowing into the electrolytic capacitors C1 to Cn, wherein currents to be supplied to the transformers T1 to Tn are commutation-flattened, are shown in FIG. 6. In addition,

channels of ripple currents are shown in FIG.8. Note that FIG. 7 shows an example when being n=2.

[0010]

In the switching circuit section 51 shown in FIG. 7, a current ib1 flows into the coil winding b1 of the transformer T1 during the time that a switching transistor Q1 has been turned on. On the other hand, the current ib1 flows into the coil winding a1 of the transformer T1 during the time that the switching transistor Q1 has been turned off. The current ib1 is a charging current to return energy absorbed in the snubber circuit to the electric power source. Besides, upon an operation of the snubber circuit, a collector voltage in the switching transistor Q1 is clamped at a voltage approximately twice the voltage of the electric power source, that is, +24V.

[0011]

A current ic1 also flows into the electrolytic capacitor C1 for supplying electric power to be consumed at the output side of the transformer T1, in addition to the currents ia1 and ib1. However, since the current ic1 is very small in comparison with the currents ia1 and ib1, the most of the ripple currents is occupied with the currents ia1 and ib1.

[0012]

The explanation was made above by taking the switching circuit section 51 as an example, however, the above-described explanation can be likely applied to the switching circuit sections 52 and 53, independently.

[0013]

Wave forms of the respective ripple currents flowing into the respective electrolytic capacitors C1 to Cn are shown in

FIG. 6(A), and summed wave form of the respective ripple currents when being n=2 is shown in FIG. 6(B). Since ripple currents each having the same phase and the same frequency flow in the respective electrolytic capacitors, a summed ripple current value when being n=2 (FIG. 6(b)) increases to a value twice a value of a single ripple current when being n=1.

[0014]

[Problem to be solved by the Invention]

However, in the conventional transformer drive circuit as shown in FIG. 5, the currents ia1 to ian and the currents ib1 to ibn have respectively flowed at the same frequency and in the same phase into the respective electrolytic capacitors C1 to Cn to thereby increase a ripple current value that is a summed value of the currents flowing into the respective electrolytic capacitors C1 to Cn since a plurality of transformers are driven based on the same clock signal.

[0015]

That is, in the conventional transformer drive circuit, the ripple current basically comes to a value several times greater than the values fixed for the switching circuit sections 51 to 53. As a result, an electrolytic capacitor having a relatively large capacity is required to be provided for the respective switching circuit sections 51 to 53.

[0016]

The present invention has attempted to solve the above-mentioned problem, and it is an object of the present invention to provide a transformer drive circuit with which, even when a plurality of switching circuit sections are installed, the sum of ripple current values flowing into electrolytic

capacitors constituting the respective switching circuit sections does not increase so as to exceed the ripple current value in the case of installing one switching circuit section, and that can be operated with a minimum requisite capacity of electrolytic capacitors.

[0017]

[Means for solving the Problem]

In order to achieve the above-described object, it is provided a separately-excited transformer drive circuit for excitingly driving a plurality of transformers according to claim 1 for the present invention characterized by comprising;

a plurality of transformers each being connected to one electric power source,

a plurality of capacitors being installed correspondingly to the plurality of transformers, each performing the commutation and smoothing of a voltage to be inputted to the corresponding transformer and performing energy supply and storage to/from the corresponding transformer,

switching transistors respectively installed correspondingly to the plurality of transformers to drive the corresponding transformer,

a clock generating means for generating at least one clock signal, and

a timing control means for generating a plurality of clock signals, phases of those which being different from one to another, based on the clock signal generated by the clock generating means.

[0018]

Further, according to the invention defined in claim 2,

the transformer drive circuit is characterized in that said clock generating means generates one clock signal, and said timing control means equally divides the cycle T of the transformer drive into n portions to obtain a time period of T/n and delays the clock signal stepwise by the time period of T/n to produce n pieces of clock signals and supplies the divided signals to the respective corresponding switching transistors.

[0019]

According to the invention defined in claim 3, said clock generating means is characterized by generating a plurality of clock signals whose phases are different from one to another.

[0020]

Further, according to the invention defined in claim 4, the transformer drive circuit is characterized in that the respective high voltages generated by the plurality of transformers are supplied to the image forming apparatus.

[0021]

[Embodiments]

The embodiments for the present invention will now be explained in the following with referring to appended drawings.

[0022]

(First Embodiment)

FIG. 1 is a circuit diagram showing the schematic configuration of the transformer drive circuit according to the first embodiment for the present invention. This transformer drive circuit supplies a high voltage to the image forming apparatus.

[0023]

In this figure, the transformer drive circuit comprises

n pieces of switching circuit sections (1 to n) 11 to 13, wherein n is a integer of 2 or more, to be separately excited and being provided independently, a clock generator 14 and a timing generator 15.

[0024]

The switching circuit section (1) 11 comprises a transformer T1, a diode D1, an electrolytic capacitor C1, a switching transistor Q1 and the others. The switching transistor Q1 is turned on and off in accordance with a clock signal inputted to a base to block conduction of a current to be supplied from an electric power source to the transformer T1. The input coil winding side of the transformer T1 is formed in a bifilar winding, and a snubber circuit is formed with the diode D1 and a coil winding a1. The common terminal of the input coil windings is connected to the electric power source (+24V) and the electrolytic capacitor C1, and the electrolytic capacitor C1 performs the commutation and smoothing of a current to be supplied to the transformer T1 and performs the supply and storage of energy to/from the transformer T1.

[0025]

The switching circuit sections (2 to n) 12 to 13 are configured likely to the switching circuit section (1) 11 and performs the same operations.

[0026]

The clock generator 14 generates a clock signal with a prefixed frequency and duty. The timing generator 15 generates display signals in a cycle at an interval of the time obtained by dividing the transformer drive cycle in accordance with the number of the switching circuit sections 11 to 13 and output

clock signals starting from the identical phase position at every timings of generating the display signals in turn to the switching circuit sections 11 to 13. Namely, the timing generator 15 delays stepwise the clock signals generated by the clock generator at every cycle period of T/n to generate n pieces of clock signals and then output the generated clock signals respectively to the corresponding switching circuit sections 11 to 13. At this time, the phases of the clocks to be supplied to the switching circuit sections (m) are represented by an equation of $\{\varphi+360°\times (m-1)/n\}$. Note that m is an arbitrary integer meeting an expression of $1 \leqq m \leqq n$. In the following explanation m is used as defined here.

[0027]

FIG. 2 contains graphs showing the wave forms of ripple currents flowing into the electrolytic capacitors when the switching circuits (m) are independently driven in response to clock signals whose phases are represented by an equation, $\{\phi+360° \times (m-1)/n\}$. Provided, for convenience's sake, it is assumed that only the capacitors Cm are connected.

[0028]

The cycle of the ripple current is represented by T. The delayed time of clock signals inputted into the switching circuit sections (m) caused by the timing generator 15 may be represented by an equation, $(m-1)\times T/n$, with reference to the clock signal inputted into the switching circuit section (1).

[0029]

Graphs showing the summed wave forms of ripple currents flowing into the respective electrolytic capacitors when being n=2, 3 or 4 are respectively shown in FIG. 3. Note that FIGS.

2 and 3 are illustrated in the same scale.

[0030]

In the conventional transformer drive circuit, the summed ripple current when being n=2 [FIG. 6(B)] was approximately twice the ripple current when being n=1 [FIG. 6(A)]. In this embodiment, however, the ripple current value when being n=2 [FIG. 3(A)] shows almost no change in comparison with the ripple current value when being n=1 [FIG. 2], though the cycle of ripple current to flow is changed to T/2. The ripple current value when being n=3 reversely decreases since the cycle of ripple current flow comes to T/3. The ripple current value when being n=4 further decreases since the cycle of ripple current flow comes to T/4.

[0031]

That means, according to this embodiment, it is possible to make the sum of the ripple currents flowing into the electrolytic capacitor Cm to be less than the current value when being n=1 since the cycle comes to T/n when the transformer drive circuit is configured with n pieces of switching circuit sections. Moreover, the ripple current value further decreases with increasing the number of n.

[0032]

Now, an explanation will be given why the sum of the ripple currents decreases.

[0033]

The currents flowing into the respective transformers Tm and the respective electrolytic capacitors Cm (m is an arbitrary integer meeting an expression of $1 \leqq m \leqq n$) when being n=2 are shown in FIG.4. Since the phases of the clock signals to be supplied

to the respective switching circuit sections (m) are represented by an expression, $\{\phi+360^\circ \times (m-1)/n\}$, the phases of respective signal supplied to the switching circuit section (1) 11 and the switching circuit section (2) 12 are given as ϕ and $\phi+180^\circ$, respectively. Therefore, these phases are deviated by 180° to each other.

[0034]

Accordingly, the respective switching transistors Qm constituting the respective switching circuit sections (m) alternately repeat turning on and off operations at different timings, and a part of the current ib1 that flows when the switching transistor Q1 has been turned on is supplied from the current ia2 that flows when the switching transistor Q2 has been turned off. Further, a part of the current ia1 that flows when the transistor Q1 has been turned off is supplied to the current ib2 that flows when the switching transistor Q2 has been turned on.

[0035]

That is, it is made possible with the transformer drive circuit according to the present invention to average the ripple currents of the overall electrolytic capacitors by providing a time lag (a phase) to the respective ripple currents, those which had been flowing at the same phase and frequency in the past.

[0036]

(Second Embodiment)

FIG. 8 is a circuit diagram showing a schematic configuration of the transformer drive circuit according to this embodiment.

[0037]

In the second embodiment, likely to the first embodiment, the transformer drive circuit comprises switching circuit sections (1 to n) 51 to 53, a clock generator 54 and a timing generator 55.

[0038]

The clock generator 54 produces k pieces of clock signals having different frequencies and duties from one to another (k is an arbitrary natural number). The timing generator 55 generate a display signal at every cycle obtained by dividing a transformer drive cycle Tj by L (L is an integer of 2 or more) and outputs the respective clock signals to the respective switching circuit sections at the generating timing of the display signals. At these outputs, the phases of clocks supplied to the respective switching circuit sections (m) (m is an integer that meets an expression of $1 \leqq m \leqq n$) are represented by any of $\{\phi + (0^\circ$ to $360^\circ)$. The cycle of the ripple current is represented by Tj (j is an arbitrary integer that meets an expression of $1 \leqq j \leqq k$).

[0039]

In the conventional high-voltage generation apparatus, the summed ripple current value when being n=2 [FIG. 6(B)] was approximately twice the ripple current when being n=1 [FIG. 6(A). According to this embodiment, however, the phase of the ripple current that flows into the respective electrolytic capacitors Cm can be arbitrarily fixed. As a result, the respective cycles Tj and phases can be fixed at will so that the sum of the values of ripple current flowing into the electrolytic capacitor Cm comes to be less than the ripple current value when being n=1.

Further, with this embodiment, it is made possible to possess a plurality of ripple currents having the same phase as well as to avoid the cycle of the ripple current from being too fast.

[0040]

That is, it is made possible with the transformer drive circuit according to the present invention to average the ripple currents of the overall electrolytic capacitors by providing a time lag (a phase) to the respective ripple currents, those which had been flowing at the same phase and frequency in the past.

[0041]

[Advantageous Effect of the Invention]

As explained above, according to the present invention, it is possible, when the transformer drive circuit is configured with n pieces of switching circuit sections (1 to n), to render the sum of the values of the ripple currents flowing into the electrolytic capacitors Cm ($1 \leqq m \leqq n$) in the switching circuit sections (m) to be less than the ripple current that flows into the electrolytic capacitor C1 when being n=1 and to further decrease the sum of the ripple current values by increasing the number of n.

[0042]

That is, it is made possible with the present invention to average the ripple currents flowing into the overall electrolytic capacitors by providing a time lag to the respective ripple currents, those which had been flowing at the same phase and frequency to the respective electrolytic capacitors in the past and to accordingly decrease the required capacity for the electrolytic capacitor and lower the cost for the transformer

drive circuit.

[Brief Explanation of the Drawings]

[FIG. 1] A circuit diagram showing a schematic configuration of a transformer drive circuit according to the first embodiment for the present invention.

[FIG. 2] Graphs respectively showing wave forms of ripple currents flowing into electrolytic capacitors Cm when switching circuits (m) are independently driven in response to signals having phases given by an expression of $\{\phi+360^{\circ} \times (m-1)/n\}$.

[FIG. 3] Graphs respectively showing summed wave forms of ripple currents flowing into respective electrolytic capacitors when being n=2, 3 and 4.

[FIG. 4] A diagram showing channels of currents flowing into electrolytic capacitors.

[FIG. 5] A block diagram showing a transformer drive circuit of the conventional type to be used in an image forming apparatus.

[FIG. 6] Graphs respectively showing wave forms flowing into capacitors and summed wave forms of currents flowing into respective capacitors when respective switching circuit sections shown in FIG. 5 are independently operated.

[FIG. 7] A diagram showing channels of currents flowing into respective capacitors shown in FIG. 5.

[FIG. 8] A circuit diagram showing a schematic configuration of the transformer drive circuit according to the second embodiment.

[Explanation for Reference Signs]

11-13: Switching circuit section (1 to n)

14: Clock generator (Clock generating means)

15: Timing generator (Timing controlling means)

C1-Cn: Electrolytic capacitor

Q1-Qn: Switching transistor

T1-Tn: Transformer